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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,871	08/31/2000	Kevin G. Donohoe	11675.185	4467

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JESUS JUANOS I TIMONEDA
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UT 84111

EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	7

DATE MAILED: 06/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,871	DONOHOE ET AL.	
	Examiner	Art Unit	
	LAN VINH	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-27 and 29-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-27 and 29-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 25, 41-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Hanazaki et al (US 6,287,980)

Hanazaki discloses a method for dry etching semiconductor substrate. This method comprises the steps of:

providing an etch treatment chamber and a semiconductor/microelectronics substrate disposed in the chamber (fig. 1)

pulsing into the etch chamber CHF_3 gas for forming a deposit on portion of the semiconductor substrate (col 26, lines 33-35; fig. 13) reads on pulsing into the etch chamber a carbon containing polymer gas suitable for forming a deposit on the substrate since CHF_3 gas is defined as carbon containing polymer gas in the specification, fig. 13 A depicts the pulsing of the etchant gas varies with the flow rate for a plurality of period of times

etching the semiconductor/microelectronics substrate with pulsing gas (col 26, lines 16-19)

Regarding claim 25, Hanazaki discloses forming a nitride layer on the substrate (col 25, lines 30-31)

Regarding claim 42, Hanazaki discloses flowing nitrogen into the chamber (col 26, lines 30-31)

Regarding claim 43, Hanazaki discloses forming a oxide/thermal oxide layer 51 on the silicon substrate/layer (col 16, lines 30-31)

Regarding claim 44, since fig. 6B of Hanazaki shows that oxide layer 51 is not etched during the etching step it reads on etching stops/halts on the oxide layer.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-9, 11-12,15,17-22, 24, 26, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanazaki et al (US 6,287,980) in view of Kumihashi et al (US 5,368,685)

Hanazaki discloses a method for dry etching semiconductor substrate. This method comprises the steps of:

providing an etch treatment chamber and a semiconductor/microelectronics substrate disposed in the chamber (fig. 1)

pulsing into the etch chamber CHF_3 gas (col 26, lines 33-35; fig. 13), fig. 13 A depicts the pulsing of the etchant gas varies with the flow rate for a plurality of period of times

etching the semiconductor/microelectronics substrate with the pulsing gas (col 26, lines 16-19)

forming a deposit with the gas on a sidewall of the microelectronics substrate over aluminum alloy film 52 (fig. 6A), the deposit prevent the sidewall of the aluminum alloy film 52 from transverse etching (side etching) (col 16, lines 46-48) reads on forming a deposit with the gas on a side surface of the microelectronics substrate, the deposit prevents additional etching of the side surface of the microelectronics substrate underneath the deposit.

Unlike the instant claimed invention as per claim 5, Hanazaki does not specifically disclose that pulsing the gases provides for the alternating steps of etching and forming/depositing on the substrate.

However, Kumihashi discloses a dry etching method comprises the step of pulsing the gas for the alternating steps of etching and depositing on the substrate (col 14, lines 48-50, col 16, lines 61-65 and fig. 9)

Since both Hanazaki and Kumihashi are concerned with dry etching using pulsing Gas, one skilled in the art would have found it obvious to employ Hanazaki's pulsing gas to alternatively etch and deposit on the substrate in view of Kumihashi's teaching

especially since Kumihashi teaches that pulsing the gas to alternatively etch and deposit on the substrate restrains a "microloading effect" (col 16, lines 59-61)

Regarding claim 6, Hanazaki discloses using high density plasma chamber/etching tool (col 24, line 20)

Regarding claim 7, Hanazaki discloses forming a silicon oxide layer/film (col 16, lines 31-32)

Regarding claims 8-9, fig. 13 A shows that the etchant gas is pulsed so that the gas is turned on and off in a plurality of period of time that reads on pulsing the gas so that the gas reaches/does not reach steady state concentration in the chamber.

The limitation of claim 11 has been discussed above.

Regarding claim 12, Hanazaki discloses flowing a second gas of nitrogen into the chamber (col 26, lines 30-31)

Regarding claim 15, Hanazaki discloses using a piezoelectric valve to control the pulse gas valve (col 14, lines 54-55)

Regarding claim 17, Hanazaki discloses forming a patterned resist layer 53 on the silicon substrate (col 16, lines 33-35 and fig. 6A)

Regarding claim 18, Hanazaki discloses forming an oxide layer 51 and nitride layer on the substrate (col 17, lines 52-54)

Regarding claim 19, fig. 6B of Hanazaki shows the etching stops on silicon layer

Regarding claims 20-21, Hanazaki discloses flowing etchant into the chamber (col 26, lines 4-5)

Regarding claim 22, Hanazaki discloses the etchant gas removes a portion of oxide layer 56 (col 26, lines 24-33 and fig. 8B)

Regarding claim 24, Hanazaki's oxide layer 51 reads on the BPSG layer

Regarding claim 26, since it is known in the art that titanium nitride and silicon nitride are equivalent nitrogen rich film (see prior art of record for evidence of this basis), one skilled in the art would have found it obvious to substitute Hanazaki's titanium nitride with silicon nitride because the substitution of one for the other would have been anticipated to produce an expected result.

Regarding claim 39, the use of oxygen in a dry etching method using pulsing gas has been discussed in Kumihashi.

5. Claims 10, 13, 14, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanazaki et al. (US 6,287,980) in view of Kumihashi et al (US 5,368,685) and further view of the following:

Hanazaki as modified by Kumihashi has been described above in paragraph 4. Unlike the instant claimed inventions as per claims 10, 13, 14, 16, Hanazaki and Kumihashi does not specifically disclose the specific duty cycle, flow rate, etch selectivity ratio. However, in a method of pulsed plasma etching , etching parameters such as duty cycle, flow rate affect the amount of material removed from the substrate by etching/etch selectivity ration (see prior art of record for evidence of this basis). It would have been obvious to adjust the flow rate, duty cycle by optimizing the same by

conducting routine experimentation for the purpose of obtaining the best etch selectivity ratio.

6. Claims 27, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanazaki et al. (US 6,287,980) in view of Lu et al. (US 5,429,978)

Hanazaki discloses a plasma processing method comprises the steps of:

disposing a patterned semiconductor substrate in a high density plasma chamber, the substrate comprising a silicon layer, an oxide layer (col 16, lines 29-32 ; col 24, line 20)

etching to remove portion of oxide layer 56 by pulsatively introducing CF_4/ fluorocarbon into the chamber (col 26, lines 24-33) ; the flow rate of CF_4 gas varies for a plurality of time as the gas is pulsed (fig. 13A), the fluorocarbon gas forms C-H deposits/protective layer (col 26, lines 66-67).

providing CHF_3 gas (col 26, lines 25-26) reads on providing a hydrofluorocarbon

Unlike the instant claimed invention as per claim 27, Hanazaki does not specifically disclose the substrate comprises a gate structure being encapsuled by SiN.

However, Lu discloses a method of forming a self-aligned stack comprises the step of etching a gate stack structure encapsuled by SiN using fluorocarbon etchant (col 4, lines 16-25)

Since Lu discloses etching a gate stack structure using the same etchant as Hanakaki, it would have been obvious to modify Hanazaki by forming a gate stack structure on the substrate as per Lu because Hanazaki is not particular about the type

of structure formed on the substrate; therefore, any structure includes a gate stack structure would have been anticipated to produce an expected result.

Regarding claim 29, Hanazaki discloses pulsing the gas of CHF_3 into high density etch chamber for a plurality of period of time (col 26, lines 32-35)

Regarding claim 30, Hanazaki discloses discloses pulsing the etchant with a piezoelectric valve (col 14, lines 54-55)

7. Claims 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanazaki et al. (US 6,287,980) in view of the following:

Hanazaki discloses a plasma processing method comprises the steps of:

forming a photoresist pattern on a semiconductor substrate includes an oxide layer and a TiN/nitride layer disposed on a silicon layer (col 16, lines 29-40; col 23, lines 33-35)

disposing the substrate in an etch chamber (col 16, lines 9-10); pulsing CHF_3 (halogenated hydrocarbon gas) into the etch chamber to form a deposit of an oxide film on the substrate (col 25, lines 30-31; col 26, lines 19-21)

fig. 13 A depicts the pulsing of the gas varies with the flow rate for a plurality of period of times

introducing the time varying flow rate of CHF_3 into the chamber in the range of 10 sccm (col 23, lines 65-66)

etching the semiconductor substrate with a pulsed CF_4/fluorocarbon gas/second gas (col 26, lines 26-30), etching to remove portion of oxide layer 56 by pulsatively

introducing CF_4/ fluorocarbon into the chamber, the etching stops on the silicon layer (col 26, lines 24-33 and fig. 8B)

Unlike the instant claimed inventions as per claim 31, Hanazaki does not specifically disclose the specific flow rate, duty cycle range. However, in a method of pulsed plasma etching, etching parameters such as duty cycle, flow rate affect the amount of material removed from the substrate (see prior art of record for evidence of this basis). Hence, it would have been obvious to adjust the duty cycle by optimizing the same by conducting routine experimentation for the purpose of obtaining the best etching rate.

Regarding claims 32-33, fig. 13A of Hanazaki shows that the etchant gas is pulsed so that the gas is turned on and off in a plurality of period of time that reads on pulsing the gas so that the gas reaches/does not reach steady state concentration in the chamber.

Regarding claim 34, Hanazaki discloses flowing nitrogen and oxygen gases into the chamber (col 22, lines 1-3).

8. Claims 23, 35-38,40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanazaki et al. (US 6,287,980) in view of Nguyen et al (US 5,933,759)

Hanazaki discloses a method for dry etching semiconductor substrate. This method comprises the steps of:

exposed a substrate to a plurality of gases (col 26, lines 15-18), pulsing into the etch chamber one of the gases (CHF_3) (col 26, lines 33-35; fig. 13 A) fig. 13 A depicts

the pulsing of the gas varies with the flow rate for a plurality of period of times, one of the gases is an etchant (CF_4), one of the gas (CHF_3) forms deposit/protective layer (col 26, lines 66-67)

Unlike the instant claimed invention as per claim 35, Hanazaki does not specifically disclose that the gas for deposit protective layer (CHF_3) is a polymer forming gas.

However, Nguyen, in a method for dry etching, discloses that carbon fluorine containing gases form polymer protection layer during etching (col 6, lines 60-63)

Hence, one skilled in the art would found it obvious that Hanazaki CHF_3 gas would have formed a polymer protection layer during etching in view of Nguyen's teaching because Nguyen states that carbon-fluorine based etchant deposits a polymer layer on the surface of the semiconductor during etching (col 5, lines 37-39)

Regarding claims 23, 38, the limitation regarding the protective layer comprises a polymer" has been discussed above.

Regarding claims 36, 40, Hanazaki discloses using BCl_3 gas (col 21, lines 27-28)

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Heinecke et al (US 4,935,661) discloses pulsed plasma etching using variables/parameters such as duty cycle, flow rate (col 6, lines 18-30)

Lyons et al (US 6,183,938) discloses that titanium nitride,silicon nitride are nitrogen rich film (col 3, lines 7-9)

Response to Arguments

10. Applicant's arguments with respect to claims 5-27,29-44 have been considered but are moot in view of the new ground(s) of rejection.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAN VINH whose telephone number is 703 305-6302. The examiner can normally be reached on Monday-Friday 8:30 -6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BENJAMIN L UTECH can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

LV
June 9, 2002